Notice of Allowability	Application No.	Applicant(s)	
	10/807,135	SASE, ICHIRO	
	Examiner	Art Unit	
	LUN-YI LAO	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *application filed on 3/24/2004*.

2. ☒ The allowed claim(s) is/are *1-4*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 3/24/2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. The following is an examiner's statement of reasons for allowance.

Applicant admitted prior art teaches a liquid crystal driving semiconductor chip comprising: a control section(30); a drive section(70S or 70C); a power-supply electrode(11) and a control electrode(13) to be applied with a control signal to enable an operation of the control section(30)(see figure 2a and paragraphs 8-12).

Yokota et al(6,633,274) teach an LCD display comprising a control section; a drive section(14, 16); a power-supply electrode(Vcc) and a control electrode(E or RS) to be applied with a control signal to enable an operation of the control section(see figure 1).

Ishimau(5,532,718) teach an LCD display comprising a control section(9); a drive section(11); a power-supply electrode(7)(see figure 3).

None of cited references teach an LCD display comprising a monitor electrode(19) which is supplied with a power supply potential of a power supply circuit in a path different from a path for the power supplied from the power supply circuit; a CMOS inverter(24) which detects a logical level of the control signal to be supplied to a control electrode(13); and a level monitor section(90) which has an MOS Transistor(93) for detecting a logical level of said power supply potential to be supplied to the monitor electrode(19), outputs a detection signal from said CMOS inverter(24) to the control section(90) as the operation control signal when the MOS transistor detects a correct logical level, and stops outputting the operation

control signal when the MOS transistor(93) does not detect the correct logical level(see figure 3), with all other limitations cite in claims 1 and 4.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi, Lao whose telephone number is (571) 272-7671.

September 4, 2006

Lun-yi Lao
Primary Examiner